Adaptive Real-Time Fault Diagnosis System For Railway Track Circuits Using Multi-Section Joint Analysis and Hierarchical Diagnosis Method

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SUMMARY

Railways are expected to operate with ever increasing levels of availability, reliability, safety and security. One way of ensuring high levels of dependability is through real-time fault detection and diagnosis. This paper presents the results of research on fault detection and diagnosis methods for railway track circuits. The proposed method uses hybrid method combing the model-based approach and the pattern recognition approach. Such a hybrid fault detection and diagnosis method combines the benefits of both approaches, i.e. the ability to analyse failure mechanism of the system and to realize the hierarchical location of the fault.

According to the fault test results on the laboratory test rig of ZPW-2000S jointless track circuit, it is shown that the proposed method can achieve the positioning accuracy of the fault section and the five rough faulty areas of the track circuit up to 99 percent, and the positioning accuracy of the 11 fine faulty areas up to 98 percent, the fault positioning accuracy of the signal cable at the transmitting end is within plus or minus 500 meters.

1 INTRODUCTION

The track circuit is the most common method for train detection. Its correct operation is critical to obtaining dependable train operations in most main line and metro systems. The track circuit is a safety device designed according to a fail-safe mechanism. However, this fail-safe property can result in significant train delays to occur if the system becomes faulty or fails altogether (Panja and Ray, 2007).

Track circuits generally use a scheduled maintenance regime: inspection is carried out on every track circuit periodically and inspection recordings are analysed visually in order to detect major defects, the disadvantages of which are higher cost, longer time and difficulty in maintenance (Roberts et al., 2002). In this case, the track circuit fault detection and diagnosis technology (referred as FDD) are proposed to overcome the shortcomings of manual fault diagnosis and improve the ability of fault detection and diagnosis, including neuro-fuzzy systems (Chen et al., 2008), Dempster–Shafer classifier fusion (Oukhellou et al., 2010), model analysis and case Study (Yang et al., 2015), AOK-TFRs and AGA (Zhao et al., 2012), and combined model (Yang et al., 2012; Gen et al., 2014).

However, the process monitoring of the track circuit FDD system is a continuous real-time task of recognizing anomalies in the process (Gertler, 1998; Dvorak and Kuipers, 1989). The track circuit FDD system poses several special difficulties: a) The track circuit is a dynamic system. b) Diagnosis should be performed as fast as possible while the track circuit operates. c) The FDD system should adapt to various situations of the track circuit.

According to the above, the proposed FDD system should realize real-time monitoring of the track circuit operation data and realize rapid identification of faults automatically, thereby accurately determining the nature and location of the fault.

2 CONCEPTION OF THE TRACK CIRCUIT

2.1 Track circuit composition

The ZPW-2000S jointless track circuit is composed of equipment in the signalling room and equipment on the trackside. The indoor equipment contains a transmitter (CEC board), a receiver (CRR board), 2 fictive lines (cable impedance analog device in the CLF board) and 1 orientation-board (CORZ). The transmitter transmits a signalling current in the rails at the track circuit's carrier frequency and the receiver receives the signal from the rails. The fictive lines compensate for the length of the cables, at transmission and reception side, to give them a constant theoretical value. The orientation-board allows changing the respective position of the transmitter and receiver and

of the track circuit depending on the running direction of the train on the track. All these boards are included in the DPIV rack of the BIV cabinet. One DPIV rack can contain two track circuits.

The outdoor equipment contains cables, 2 matching transformers (TAD), electrical separation joints (JES), compensation capacitors and blocking units. Cables at the transmission and the reception link the indoor equipment and outdoor equipment. The matching transformers achieve impedance matching between cables and rails. The JESs are made up of 2 tuning units (BU) and an air core inductor (SVAC) between 2 successive track circuits, which can provide the traction current return instead of insulted joints. The compensation capacitors could compensate for the high longitudinal inductance and the blocking units could compensate for the risk of a tuning unit failure.

2.2 Condition monitoring system

The condition monitoring system is responsible for collecting the parameters of the track circuit. The test position of TP1~TP9 is shown in Figure 2-1 and Table 2-1.

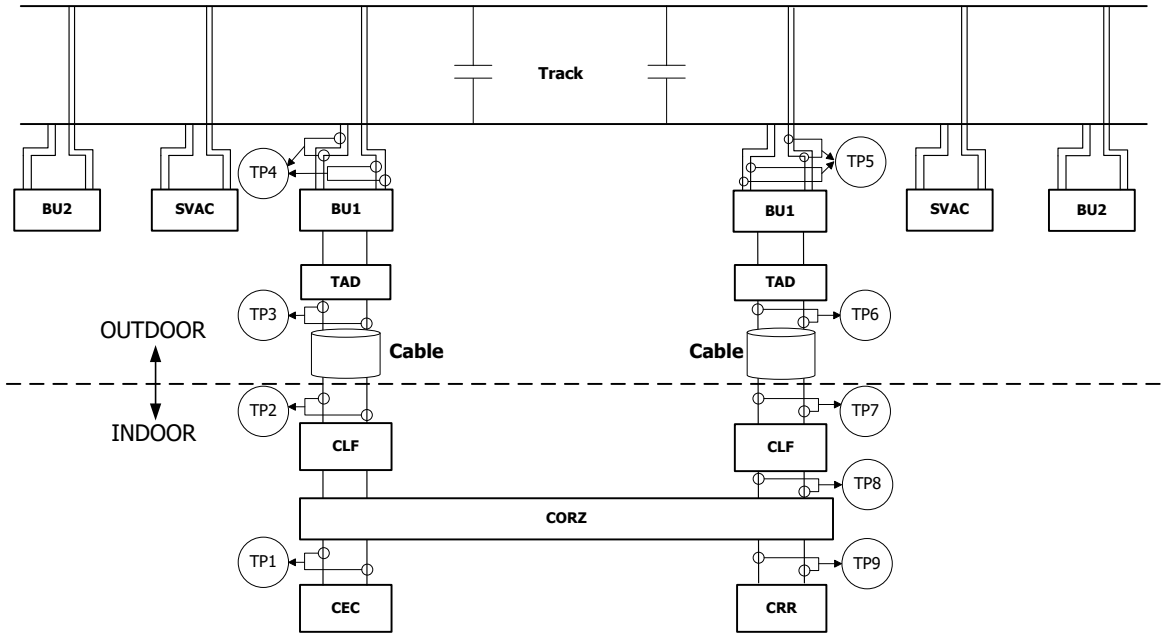


Figure 2-1: System Block of Track Circuit of ZPW-2000S

Table 2-1: Test Parameters

Test Code	Parameter	Position
TP1	Power output voltage	CEC board output port
TP1	Power output current	
TP2	Indoor cable voltage at transmission side	Between the CLF board and cable at transmission side
TP2	Indoor cable current at transmission side	
TP3	Outdoor cable current at transmission side	Between the TAD and cable at transmission side
TP 4	Rail connection wire current at transmission side	Wires between the BU and rail at transmission side
TP 5	Rail connection wire current at reception side	Wires between the BU and rail at reception side
TP 6	Outdoor cable current at reception side	Between the TAD and cable at reception side
TP 7	Indoor cable voltage at reception side	Between the CLF board and cable at reception side
TP 7	Indoor cable current at reception side	
TP 7	Indoor cable voltage at reception side	
TP 8	Main track input voltage at reception side	Between the CLF board and CORZ board at reception side
TP 8	Small track input voltage at reception side	
TP 9	Main track output voltage at reception side	Between the CRR board and CORZ board at reception side
TP 9	Small track output voltage at reception side	

2.3 Track circuit frequency alternation

The ZPW2000S track circuits use 4 frequencies from 1700Hz to 2600Hz. The safety of traffic detection by the track circuits is based on the following principle: On a given track, the adjacent track circuits operate at different frequencies; And on a double track, the track 1 track circuits operate at frequencies that are different to those of the track 2 track circuits. On track 1, V1F1=1700 Hz and V2F1=2300 Hz perform the frequency alternations; and on track 2, V2F1=2000 Hz and V2F2=2600 Hz perform the frequency alternations.

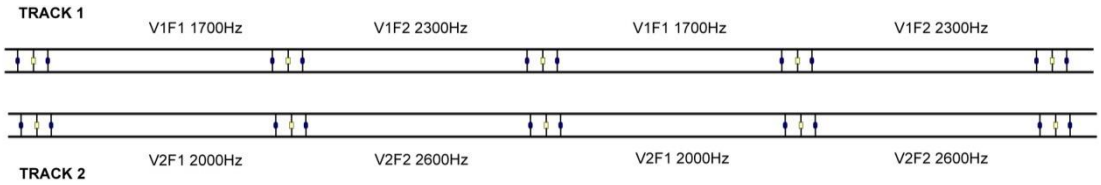


Figure 2-2: Track circuit frequency alternation

3 TRACK CIRCUIT MODEL

The jointless track circuit is a complicated system which could be simulated with software tools. In the model-based approach, firstly it is to build the track circuit model (Isermann, 2005; Dimitrova, et al., 2007).

3.1 Single-track section model

3.1.1 Track portion model

Previously, Hill and Carpenter (1993) and Berova (1997) showed that the track portion of a railway track circuit can be modelled as a transmission line, approximated by identical subsections composed of discrete passive electrical elements.

Assume the signal on one side of the transmission line: $u = u(z,t)$, $i = i(z,t)$, then the telegraph equation expression (Yan, 2006) is as follows:

$$\begin{cases} \dfrac{\partial u(z,t)}{\partial z} = -Ri(z,t) - L\dfrac{\partial i(z,t)}{\partial t} \\ \dfrac{\partial i(z,t)}{\partial z} = -Gu(z,t) - C\dfrac{\partial u(z,t)}{\partial t} \end{cases} \tag{3.1}$$

In the expression, the resistance R and inductance L represent the rail series impedance, while the conductance G and capacitance C represent the track shunt admittance.

When the signal is a sinusoidal signal: $u(z,t) = U(z)\cdot e^{jwt}$, $i(z,t) = I(z)\cdot e^{jwt}$, then the expression (3.1) is as follows:

$$\begin{cases} \dfrac{dU(z)}{dz} = -(R + jwL)I(z) = -ZI(z) \\ \dfrac{dI(z)}{dz} = -(G + jwC)U(z) = -YU(z) \end{cases} \tag{3.2}$$

In the expression, $Z = R + jwL$, $Y = G + jwC$。

Perform a Laplace transform on a $U(z)$ and $I(z)$, $V(s)$ and $J(s)$ are the results of the Laplace transform of $U(z)$ and $I(z)$.

$$\begin{cases} V(s) = \int_0^{\infty} U(z) e^{-sz} dz \\ J(s) = \int_0^{\infty} I(z) e^{-sz} dz \end{cases} \tag{3.3}$$

Perform a Laplace transform on both sides of the expression (3.3) , the result is as follows.

$$\begin{cases} sV(s) - U(0) = -Z \cdot J(s) \\ sJ(s) - I(0) = -Y \cdot U(s) \end{cases} \tag{3.4}$$

The solution to the equations (3.4) is as follows.

$$\begin{cases} V(s) = \dfrac{sU(0) - zI(0)}{s^2 - ZY} \\ J(s) = \dfrac{sI(0) - YU(0)}{s^2 - ZY} \end{cases} \tag{3.5}$$

Take the Laplace inverse transform on (3.5), the result is as follows.

$$\begin{cases} U(z) = U_0 \cosh(\gamma z) + I_0 Z_c \sinh(\gamma z) \\ I(z) = I_0 \cosh(\gamma z) + U_0 \dfrac{\sinh(\gamma z)}{Z_c} \end{cases} \tag{3.6}$$

For a two-port circuit network, when the input voltage and current are $\overset{g}{U}_{in}$ and $\overset{g}{I}_{in}$ on one side of the network and the output voltage and current are $\overset{g}{U}_{out}$ and $\overset{g}{I}_{out}$ on the other side, the transfer equation of the network is defined as follows and N is defined as the transfer matrix.

$$\begin{vmatrix} \overset{g}{U}_{in} \\ \overset{g}{I}_{in} \end{vmatrix} = \mathbf{N} * \begin{vmatrix} \overset{g}{U}_{out} \\ \overset{g}{I}_{out} \end{vmatrix} = \begin{vmatrix} A & B \\ C & D \end{vmatrix} * \begin{vmatrix} \overset{g}{U}_{out} \\ \overset{g}{I}_{out} \end{vmatrix} \tag{3.7}$$

When a system is the result two-port network cascading, then the transfer matrix of the system is defined as follows.

$$\begin{vmatrix} \overset{g}{U}_{in} \\ \overset{g}{I}_{in} \end{vmatrix} = \mathbf{N} * \begin{vmatrix} \overset{g}{U}_{out} \\ \overset{g}{I}_{out} \end{vmatrix} = \prod_{i=1}^{n} \mathbf{N}_i * \begin{vmatrix} \overset{g}{U}_{out} \\ \overset{g}{I}_{out} \end{vmatrix} \tag{3.8}$$

For track potion without any compensated capacitors and cables at transmission and reception side, the two-port network transfer matrix is as follows:

$$\mathbf{N}_{\mathbf{Track}} \left(\mathbf{or}\ \mathbf{N}_{\mathbf{Cable}} \right) = \begin{vmatrix} \cosh(\gamma \cdot l) & Z_c \sinh(\gamma \cdot l) \\ \dfrac{1}{Z_c} \sinh(\gamma \cdot l) & \cosh(\gamma \cdot l) \end{vmatrix} \tag{3.9}$$

In the expression, l is the length of the cable or the track。

For a track unit with compensated capacitor, of which the length is general 60 meters or 80 meters, the two-port network transfer matrix is as follows:

$$\mathbf{N}_{\mathbf{Track\text{-}uc}} = \begin{vmatrix} \cosh\left(\gamma \cdot \dfrac{l_u}{2}\right) & Z_c \sinh\left(\gamma \cdot \dfrac{l_u}{2}\right) \\ \dfrac{1}{Z_c} \sinh\left(\gamma \cdot \dfrac{l_u}{2}\right) & \cosh\left(\gamma \cdot \dfrac{l_u}{2}\right) \end{vmatrix} \tag{3.10}$$

In the expression， l_u is the length of the track unit。

When $\mathbf{N}_{\mathbf{C}}$ is the transfer matrix of a compensated capacitor, the two-port network transfer matrix of the track portion is as follows:

$$\mathbf{N}_{\mathbf{Track}} = \left(\mathbf{N}_{\mathbf{N}_{\mathbf{Track\text{-}uc}}} * \mathbf{N}_{\mathbf{C}} * \mathbf{N}_{\mathbf{N}_{\mathbf{Track\text{-}uc}}}\right)^{n} \tag{3.11}$$

In the expression， n is the number of the track unit。

3.1.2 Track circuit transfer matrix

From a mathematical model perspective, the system of track circuit can be divided into three parts: transmitting side portion, track portion and receiving side. The system input is defined as $\overset{g}{U}_{CEC}$ 和 $\overset{g}{I}_{CEC}$ and the system output is defined as $\overset{g}{U}_{CRR}$ 和 $\overset{g}{I}_{CRR}$.

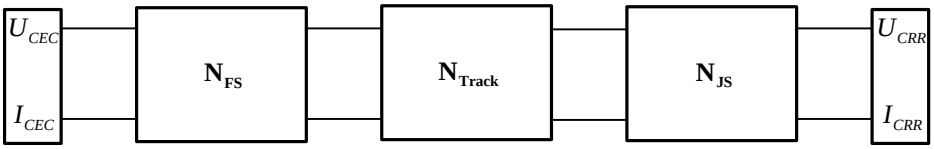


Figure 3-1: Track circuit matrix model

The system of single-section track circuit transmission matrix is as follows.

$$\begin{vmatrix} \overset{g}{U}_{CEC} \\ \overset{g}{I}_{CEC} \end{vmatrix} = \mathbf{N} * \begin{vmatrix} \overset{g}{U}_{CRR} \\ \overset{g}{I}_{CRR} \end{vmatrix} \tag{3.12}$$

Considering the system is cascaded from the three parts, the system matrix can be expressed as follows.

$$\mathbf{N} = \mathbf{N}_{\mathbf{FS}} * \mathbf{N}_{\mathbf{Track}} * \mathbf{N}_{\mathbf{JS}} = \begin{vmatrix} A_{fs} & B_{fs} \\ C_{fs} & D_{fs} \end{vmatrix} * \begin{vmatrix} A_{track} & B_{track} \\ C_{track} & D_{track} \end{vmatrix} * \begin{vmatrix} A_{js} & B_{js} \\ C_{js} & D_{js} \end{vmatrix} \tag{3.13}$$

3.2 Multi-track section model

When a single track section fails, the adjacent section may be affected. Therefore, to implement fault diagnosis of the track circuit, a multi-section model needs to be established. The multi-section contains AG track, BG track and CG track, of which BG track is set as the fault section and the other two sections are set as normal sections. The multi-section system block is shown in Figure 3-2.

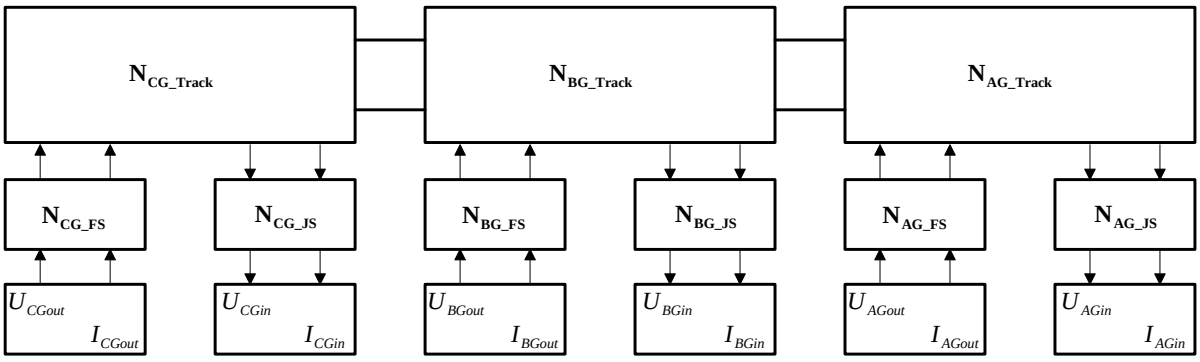


Figure 3-2: Multi-section system block

When the input and the output belong to the same section, the transfer equation is as follows.

$$\begin{vmatrix} \overset{g}{U}_{pout} \\ \overset{g}{I}_{pout} \end{vmatrix} = \mathbf{N_{pp}} \begin{vmatrix} \overset{g}{U}_{pin} \\ \overset{g}{I}_{pin} \end{vmatrix} = \begin{vmatrix} A_{pp} & B_{pp} \\ C_{pp} & D_{pp} \end{vmatrix} \begin{vmatrix} \overset{g}{U}_{pin} \\ \overset{g}{I}_{pin} \end{vmatrix} \tag{3.14}$$

When the input and the output belong to different sections, the coupling equation is as follows.

$$\begin{vmatrix} \overset{g}{U}_{pout} \\ \overset{g}{I}_{pout} \end{vmatrix} = \mathbf{N_{pq}} \begin{vmatrix} \overset{g}{U}_{qin} \\ \overset{g}{I}_{qin} \end{vmatrix} = \begin{vmatrix} A_{pq} & B_{pq} \\ C_{pq} & D_{pq} \end{vmatrix} \begin{vmatrix} \overset{g}{U}_{qin} \\ \overset{g}{I}_{qin} \end{vmatrix} \qquad , p \neq q \tag{3.15}$$

Therefore, the system of multi-section track circuit transmission matrix is as follows.

$$\begin{vmatrix} \overset{g}{U}_{AGout} \\ \overset{g}{I}_{AGout} \\ \overset{g}{U}_{BGout} \\ \overset{g}{I}_{BGout} \\ \overset{g}{U}_{CGout} \\ \overset{g}{I}_{CGout} \end{vmatrix} = \begin{vmatrix} \mathbf{N_{11}} & \mathbf{N_{12}} & \mathbf{N_{13}} \\ \mathbf{N}_{21} & \mathbf{N}_{22} & \mathbf{N}_{23} \\ \mathbf{N}_{31} & \mathbf{N}_{32} & \mathbf{N}_{33} \end{vmatrix} * \begin{vmatrix} \overset{g}{U}_{AGin} \\ \overset{g}{I}_{AGin} \\ \overset{g}{U}_{BGin} \\ \overset{g}{I}_{BGin} \\ \overset{g}{U}_{CGin} \\ \overset{g}{I}_{CGin} \end{vmatrix} = \begin{vmatrix} A_{11} & B_{11} & A_{12} & B_{12} & A_{13} & B_{13} \\ C_{11} & D_{11} & C_{12} & D_{12} & C_{13} & D_{13} \\ A_{21} & B_{21} & A_{22} & B_{22} & A_{23} & B_{23} \\ C_{21} & D_{21} & C_{22} & D_{22} & C_{23} & D_{23} \\ A_{31} & B_{31} & A_{32} & B_{32} & A_{33} & B_{33} \\ C_{31} & D_{31} & C_{32} & D_{32} & C_{33} & D_{33} \end{vmatrix} * \begin{vmatrix} \overset{g}{U}_{AGin} \\ \overset{g}{I}_{AGin} \\ \overset{g}{U}_{BGin} \\ \overset{g}{I}_{BGin} \\ \overset{g}{U}_{CGin} \\ \overset{g}{I}_{CGin} \end{vmatrix} \tag{3.16}$$

According to the Matrix distribution law, the expression (3.17) could be expressed as the following.

$$\begin{vmatrix} \overset{g}{U}_{AGout} \\ \overset{g}{I}_{AGout} \\ \overset{g}{U}_{BGout} \\ \overset{g}{I}_{BGout} \\ \overset{g}{U}_{CGout} \\ \overset{g}{I}_{CGout} \end{vmatrix} = \begin{vmatrix} \mathbf{N_{11}} & \mathbf{N_{12}} & \mathbf{N_{13}} \\ \mathbf{N}_{21} & \mathbf{N}_{22} & \mathbf{N}_{23} \\ \mathbf{N}_{31} & \mathbf{N}_{32} & \mathbf{N}_{33} \end{vmatrix} * \left[\begin{vmatrix} \overset{g}{U}_{AGin} \\ \overset{g}{I}_{AGin} \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix} + \begin{vmatrix} 0 \\ 0 \\ \overset{g}{U}_{BGin} \\ \overset{g}{I}_{BGin} \\ 0 \\ 0 \end{vmatrix} + \begin{vmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \overset{g}{U}_{CGin} \\ \overset{g}{I}_{CGin} \end{vmatrix} \right] \tag{3.17}$$

According to the expression (3.17), it is concluded that the simulation of the multi-section model could be decomposed into three steps.

4 HIERARCHICAL DIAGNOSTIC ALGORITHM

4.1 Failure area and mode

For track circuit， it could be divided into 5 rough faulty areas and the 11 fine fault areas. The 5 faulty areas are transmission channel area, tuning area at transmission side, track portion area, tuning area at reception side and reception channel area. The 5 rough faulty areas and 11 faulty areas are shown in Figure 4-1.

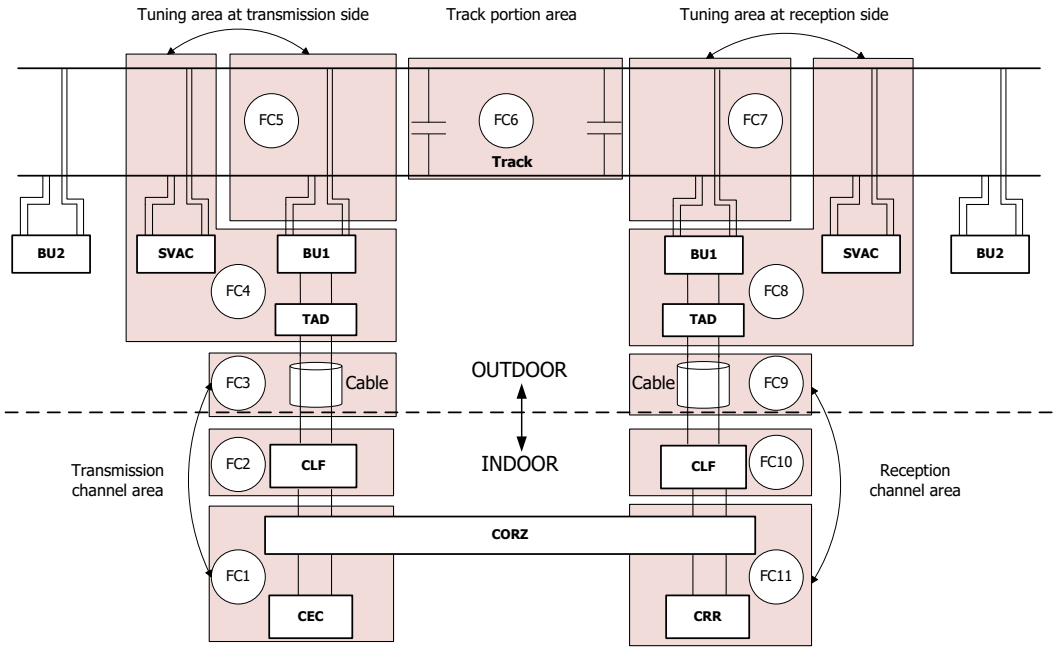


Figure 4-1: Track circuit fault area division

The 11 Faulty areas and the failure mode are listed in Table 4-1.

Table 4-1: Failure 11 areas and form

Fault Code	11 Faulty areas	Failure mode
FC0	Healthy operation	No
FC1	CORZ board at transmission side	11）Output open circuit 12）Output short circuit
FC 2	CLF board at transmission side	21）Open circuited 22）Short circuited
FC 3	Cable channel at transmission side	31）Open circuited 32）Short circuited
FC 4	Tuning area at transmission side	41）Tuning unit failure 42）SVAC failure
FC 5	Wires between the BU and rail at transmission side	51）Single disconnection 52）Double disconnection
FC 6	Track portion	61）Compensation capacitor failure
FC 7	Wires between the BU and rail at reception side	71）Single disconnection 72）Double disconnection
FC 8	Tuning area at reception side	81）Tuning unit failure 82）SVAC failure
FC 9	Cable channel at reception side	91）Open circuited 92）Short circuited
FC 10	CLF board at reception side	101）Open circuited

FC 11	CORZ board at reception side	102）Short circuited 111）Output open circuit 112）Output short circuit

4.2 Hierarchical diagnosis algorithm model

Based on the multi-track section model, the fault insertion simulation of the model was carried out to obtain the voltage and current data of the specific acquisition points when different carrier frequencies, different configurations and different fault locations were obtained. The fault data extraction diagram is shown in Figure 4-2.

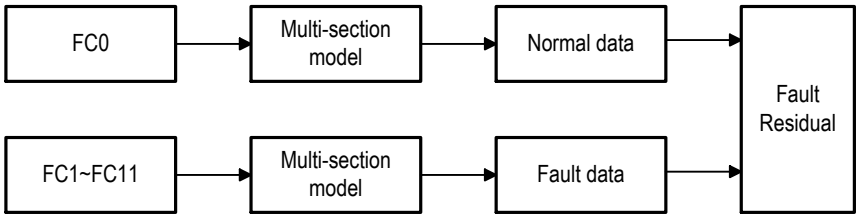


Figure 4-2: Model-based fault data extraction diagram

The hierarchical diagnosis algorithm is composed of fault section diagnosis, 5 faulty areas diagnosis, 11 faulty areas diagnosis and fault form diagnosis, as in Figure 4-3.

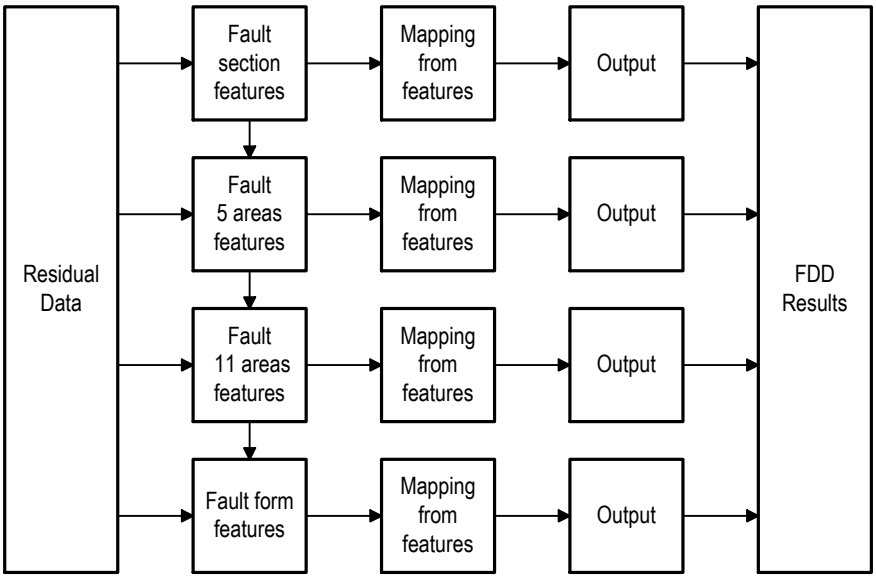


Figure 4-3: Hierarchical diagnosis algorithm model

4.3 FDD system structure

The FDD system includes condition monitoring unit, fault detection unit and the hierarchical diagnosis algorithm unit. In the system, the condition monitoring unit collects and normalizes data in real time. The fault detection unit checks whether there is failure with the track circuit while the hierarchical diagnosis algorithm unit carry out the final diagnosis of the track circuit.

5 TEST RIG AND RESULTS

5.1 Test rig

To verify the FDD system, a lab-based track circuit test rig was constructed. The test rig contains the simulated track device, the track circuit, the condition system and the fault diagnosis system. System block diagram of the test rig is shown in Figure 5-1. In the test rig, the simulated track device is consisted of AG track, BG track, CG

track and the four turning areas and the train forward direction is from AG track to CG track, as shown in Figure 5-2. The track portion connects the indoor equipment (CE_In and RE_In) and outdoor equipment (CE_Out and RE_Out) respectively. The condition monitoring system is responsible for acquiring the signal from TP1 to TP9 and the fault diagnosis system will show the diagnosis result. The test rig equipment is shown in Figure 5-3.

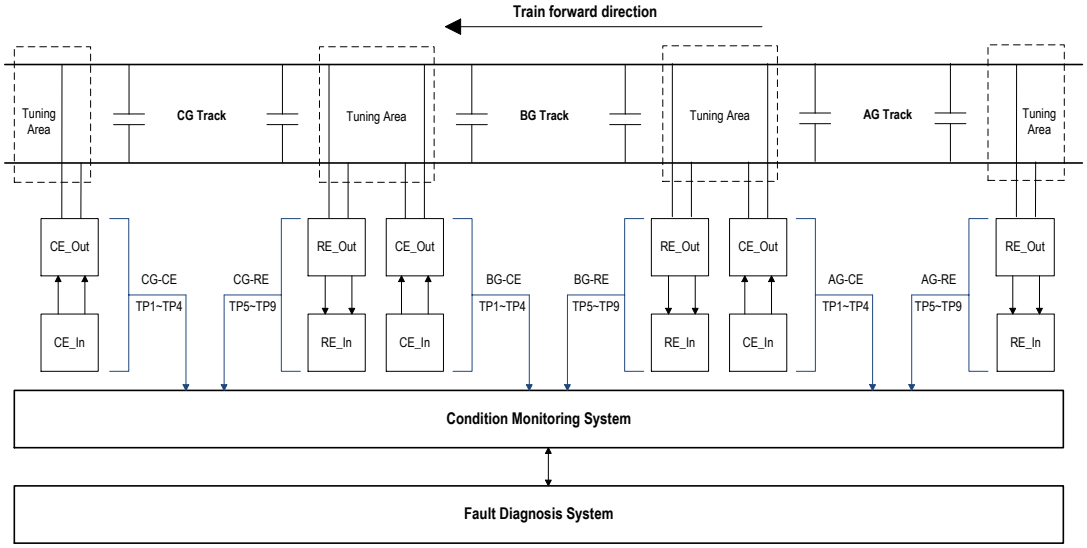


Figure 5-1: System block diagram of test rig

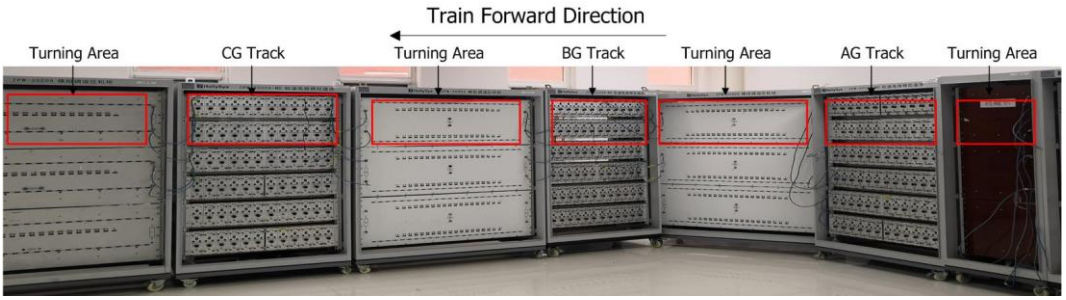


Figure 5-2: Simulated track device

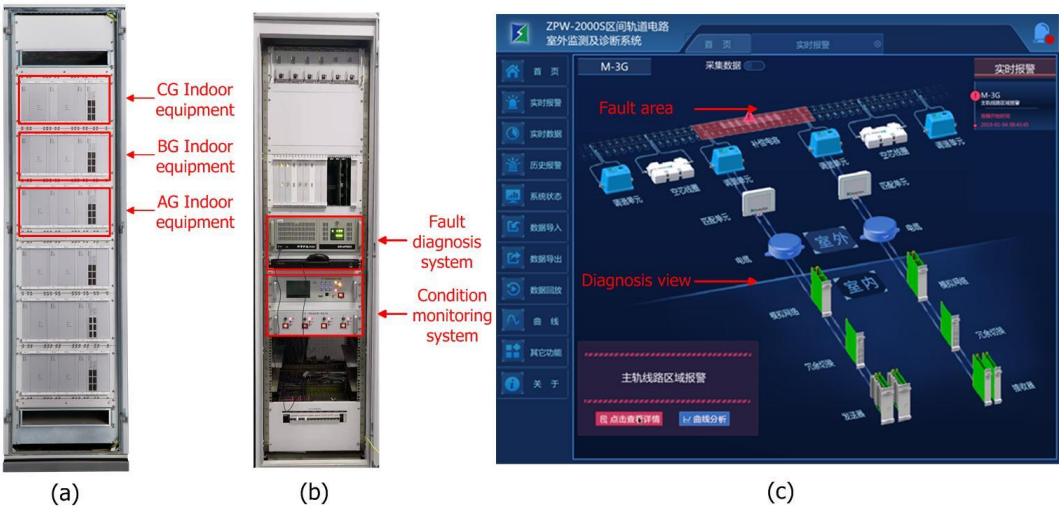
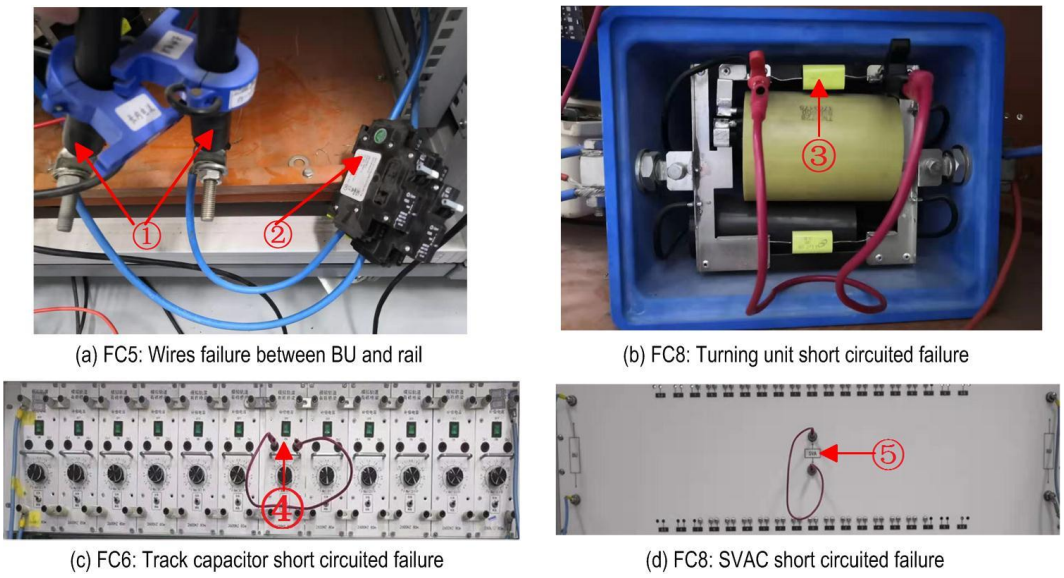


Figure 5-3: Test rig equipment: (a) ZPW-2000S Jointless Track Circuit

(b) Cndition monitoring sysytem and fault diagnosis system, (c) Fault diagnosis software interface

5.2 Fault diagnosis test

The fault diagnosis test was carried on the BG track and its front and rear turning area. 50 tests of FC1 to FC11 were carried out and the typical fault insertion method was shown in Figure 5-4. In the test, fault insertion method was consisted of short circuit failure and open circuit failure. In Figure 5-4, the meaning of component number is as following: ①Wires between the BU and rail, ②Air switches used for cutting off the wires, ③BU unit capacitor, ④Compensation capacitor position, ⑤SVAC unit.



(a) FC5: Wires failure between BU and rail

(b) FC8: Turning unit short circuited failure

(c) FC6: Track capacitor short circuited failure

(d) FC8: SVAC short circuited failure

Figure 5-4: Typical fault insertion method

The results of the FDD system are shown in Table 5-1. It is concluded that the average diagnosis accuracy was higher than 98% and the average diagnosis time was less than 11 s.

Table 5-1: Results of FDD system

Fault Code	Failure form	Diagnosis result	Diagnosis time/s
FC0	No	99.21%	/
FC1	11） Output open circuit	98.32%	11.3
	12） Output short circuit	97.53%	11.2
FC 2	21） Open circuited	96.04%	11.3
	22） Short circuited	96.33%	11.2
FC 3	31） Open circuited	99.24%	12.7
	32） Short circuited	99.58%	13.5
FC 4	41） Tuning unit failure	98.23%	11.5
	42） SVAC failure	95.66%	12.3
FC 5	51） Single disconnection	99.81%	2.2
	52） Double disconnection	98.38%	11.9
FC 6	61 ） Compensation capacitor failure	97.12%	11.6
FC 7	71） Single disconnection	99.58%	2.6
	72） Double disconnection	98.45%	11.7
FC 8	81） Tuning unit failure	99.55%	11.9

FC 9	82） SVAC failure	96.28%	12.2
	91） Open circuited	98.15%	11.3
	92） Short circuited	98.43%	11.2
FC 10	101） Open circuited	97.53%	11.6
	102） Short circuited	99.22%	11.3
FC 11	111） Output open circuit	99.35%	11.3
	112） Output short circuit	98.07%	11.4
Average	50 tests	98.18%	10.81

For the cable fault diagnosis, the fictive line is 2Km and the cable is 8Km at transmission side. When the fault position ranged from 0 Km to 8Km, the fault diagnosis results was shown in Table 5-2. Then it could be concluded the fault *positioning accuracy of the signal cable at the transmitting end is within plus or minus 500 meters.*

Table 5-2: Results of cable fault diagnosis

Position /Km	**FC3-31 /Km**	**FC3-32 /Km**
0	0~0.4	0~0.5
1	0.8~1.2	0.7~1.1
2	1.9~2.3	1.9~2.2
3	2.8~3.2	2.9~3.2
4	3.7~4.1	3.8~4.1
5	4.8~5.2	4.9~5.2
6	5.9~6.1	5.6~6.1
7	6.7~7.1	6.8~7.2
8	7.8~8.2	7.8~8.1

6 CONCLUSION

The conclusion is as follows:

（1） The proposed method used hybrid method combing the model-based approach and the pattern recognition approach, which could be a good method for other FDD systems.

（2） The FDD system for railway track circuits proposed by the paper realized on-line fault diagnosis within 15 seconds and accurate diagnosis up to 98 percent.

（3） The test rig of ZPW-2000S jointless track circuit was used to verify the FDD system. And in the future, field test should be carried out with the system.

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